GLOBAL JOURNAL OF ENGINEERING SCIENCE AND RESEARCHES

HIGH PERFORMANCE SCALABLE INPUT VECTOR MONITORING CONCURRENT BIST ARCHITECTURE

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Abstract

Built-in Self-Test (BIST) techniques are used to form an effective and practical approach for VLSI circuit testing. BIST has an advantage over cost and memory storage reduction and it can test many units in parallel. A novel input vector monitoring concurrent BIST schemes are proposed for getting either exhaustive or pseudorandom testing separately without disturbing the normal operation. This method is mainly depend on monitoring a set of vectors that is window reaching the inputs. To store the relative locations of the test vector a static RAM like structure is used. The proposed scheme is shown to have lower Hardware Overhead and Concurrent Test Latency (CTL) compared to previously proposed schemes.

Keywords: Built-in self-test, Hardware overhead, concurrent test latency, testing.

I. INTRODUCTION

Built in self test (BIST) is a design technique in which parts of a circuit are used to test the circuit itself, It does not need any extra hardware to test the circuit. Parts of a circuit that must be operational to execute a self test. BIST categories areMemoru BIST and Logic BIST. BIST Techniques are Test Pattern Generation Techniques (TPG) Test Response Compression Techniques. The BIST techniques are classified based on the operational condition of the circuit under test as On-line BIST and Off-line BIST. On-line Testing occurs during normal functional operating conditions. On-line testing includes concurrent and non concurrent. Off-line BIST deals with testing a system when it is not carrying out its normal functions. Off-line testing includes functional and structural BIST architecture is given below. Factors affecting the choice of BIST are Degree of test parallelism,Fault coverage,Level of packaging,Test time,Complexity of replaceable unit,Factory and field test-and-repair strategy,Performance degradation, and Area overhead. BIST Architecture is given below.

BIST ARCHITECTURE

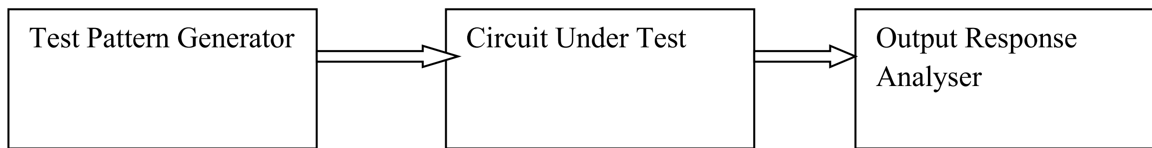

Figure.BIST Architecture

It consist of three blocks Test Pattern Generator, Circuit Under Test and Output Response Analyzer. The input data that are given to the test pattern Generator and the test pattern generator generates the test vector as a sequence of zeros and one. The testing sequence are given to the circuit under test and this sequence are compared with the output analyser or comparator to produce the testing sequence. BIST architecture does not need an extra Hardward to test the circuit and it tests with the components inside the circuit. The Architecture shows the working of Built In Self Test operation.

The major component of BIST architecture are Test Pattern Generator, Circuit Under Test (CUT), Output Response Analyser. The main advantage of this architecture is reduction in cost and storage. Moreover it can use many units in parallel. BIST architecture consist of three major sections and that are Built-in Logic Block Observsr (BILBO), Self Testing Using an MISR and Paralle Shift Register (STUMPS), and LSSD on-Chip Self-Test (LOCST).

II. RELATED WORKS

Ioannis and Coastas Efstathiou [1] have estimated input vector monitoring BIT architecture to provide the speed testing with the High Fault Coverage. BIST has an effective solution to the problem of testing the VLSI devices. BIST techniques are classified into on-line and off-line testing. Offline architecture can operate either in normal or in test mode. In test mode the generated inputs are applied to the circuit under test and its output is captured into the response versifier.

In order to perform the test, the normal mode of operation of the circuit has to be stopped which will degrade the performance of the CUT. To avoid this performance degradation a novel input vector monitoring concurrent BIST technique are proposed. The proposed technique improves the testing activities and to reduce hardware overhead and Concurrent Test Latency (CTL) with previously proposed schemes with respect to hardware overhead and CTL tradeoff. For example if proposed scheme has CTL equals to 3sec it required 761 gates othes schemes SWIM needs 898 gates it is 16% more than proposed scheme, and W-MCBIST requires 1136 gates and it is 33% more, R-CBIST requires 1553 gates and it is 102% more than the proposed scheme.

R.Sharma and K.K.Saluja [2] have used a novel technique called Built In Concurrent Self Test (BICST). The underlying resources of off-line testing are modified to use for both off-line and on-line testing. By operating in normal mode

concurrently, it can shown be that BICST circumvents the degradation caused by the periodic maintenance of testing. Comparison between BICST and self-checking circuit the self checking circuit provide 100% protection than BICST against errors occurred in transient fault. Self-checking circuits ia commonly a single stuck at fault and it is a model-secure at all times. It also provides enhanced diagnostic capability along with reduction in the system maintenance requirements. It can detect various faults such as transient, intermittent and permanent faults.

I.Voyiatzis, A.Paschaslis, D.Gizopoulos, N.Kranitis, and C.Halastzis [3] have implemented RAM based input vector monitoring concurrent BIST (R-CBIST) for the continuous testing of combinational circuits. Though this method results in high concurrent test latency, this has got low hardware overhead. For CTL value less than !sec, with the percentage hardware overhead less than 12% and with the operating speed 133MHZ. In addition to this, Multiple Hardware Signature Analysis (MHSAT) is also applied for the testing process.

I. Voyiatzis, D. Nikolos, A. Paschalis, C. Halatsis, and T. Haniotakis [4] have made use of order independent signature analysis technique, windowed comparative concurrent BIST (W-BIST) technique to drive down the latency with an increase in the number of active test vectors.

I. Voyiatzis, and C. Halatsis [5] have applied a novel input vector monitoring concurrent BIST scheme termed as Window-Monitoring Concurrent BIST (W-MCBIST). In this paper percentage hardware overhead is less than 10% and HO% equals to 3,65% and CTL equals to 1,82sec. If less than 2sec CTL equal to 3sec and hardware overhead required by W-MCBIST needs 1,150 gates and for BCIST needs 1,550 gates. It drives down the value of effective CTL to a required level and also the aliasing probability which will exploit the concept of multiple signature examination.

Vishal Suthar and Shantanu Dutt[6] have developed a strong BIST scheme named as Roving Star. Also, they have presented Mixed and Interleaved BIST (M-BIST, I-BIST) assuming the circuit as fault-free.In this method the system is able to achieve very high diagonisability of 98.5 to 100% in present of high fault densities upto 16% and also clustered faults. This method is efficient in testing a circuit and has high fault density across the interconnects.

S.Almukhaizim, P.Drineas, and Y.Makris [7] have discussed the problem of parity-tree selection for Concurrent Error Detection (CED) with low overhead in Finite State Machine (FSM). They have developed a non-intrusive technique for CED that minimizes the number of parity tree for lossless compaction. Moreover, it reduces the area overhead and power consumption. Benchmark circuits are indicators of entropy-driven tree selection and it compares with the existing schemes to select the minimum number of parity trees.

S.Almukhaizim and Y.Makri [8] is have applied Duplication based CED, Transition Triggered CED and Berger Code-based CED. CED is a problem that occurs in asynchronous burst mode machines. In the above three methods Transition Triggered CED can have an average of only 3% over the Duplication based CED and this is sometimes more expensive. Berger Code-based CED have the average of 15% over Duplication based CED and also 11% over Transition Triggered CED. Of all the three methods, Berger Code-based CED results in low area overhead.

III. CONCLUSION

BIST techniques are used to provide a better solution for testing VLSI circuits. It aims at reducing overhead and Concurrent Test Latency (CTL). BIST architecture works on the basis of the information stored in the SRAM-cell like structure. In future, benchmark circuits can be implemented to further reduce the area overhead and latency.

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